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Three-Dimensional Flexible Complementary Metal–Oxide–Semiconductor Logic Circuits Based On Two-Layer Stacks of Single-Walled Carbon Nanotube Networks

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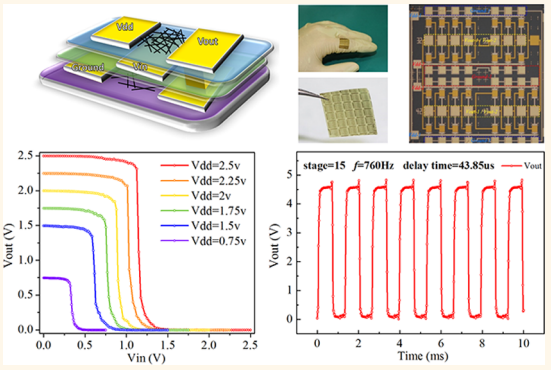
Supporting Information

ABSTRACT: We have proposed and fabricated stable and repeatable, flexible, single-walled carbon nanotube (SWCNT) thin film transistor (TFT) complementary metal–oxide–semiconductor (CMOS) integrated circuits based on a three-dimensional (3D) structure. Two layers of SWCNT-TFT devices were stacked, where one layer served as n-type devices and the other one served as p-type devices. On the basis of this method, it is able to save at least half of the area required to construct an inverter and make large-scale and high-density integrated CMOS circuits easier to design and manufacture. The 3D flexible CMOS inverter gain can be as high as 40, and the total noise margin is more than 95%. Moreover, the input and output voltage of the inverter are exactly matched for cascading. 3D flexible CMOS NOR, NAND logic gates, and 15-stage ring oscillators were fabricated on PI substrates with high performance as well. Stable electrical properties of these circuits can be obtained with bending radii as small as 3.16 mm, which shows that such a 3D structure is a reliable architecture and suitable for carbon nanotube electrical applications in complex flexible and wearable electronic devices.



KEYWORDS: *3D structure, CMOS, flexible, logic device, SWCNT, wearable*

Single-walled carbon nanotubes (SWCNTs) are promising candidates for future electronic devices because of their excellent electrical and mechanical properties, including high mobility,[1] large current density,[2] and extremely good mechanical strength.[3] In particular, because of their uniformity and repeatability, thin film transistors (TFTs) with SWCNT random networks as conductive channels have been widely studied. Meanwhile, depositing or printing preseparated semiconducting SWCNTs[4,5] or transferring networks grown by chemical vapor deposition[6] onto flexible substrates can meet the needs of flexible and wearable electronic devices. As we all know, SWCNT-TFTs show p-type characteristics in ambient conditions because of the adsorption of oxygen and water vapor.[7,8] Although many applications, such as logic circuits,[9,10] memory devices,[11] sensors,[12] or even computers,[13] are fabricated by p-type TFTs, complementary metal–oxide–semiconductor (CMOS) circuits including a couple of n-type and p-type TFTs are still demanded urgently because of their low static power consumption and large noise margin. To date, several methods have been investigated to achieve high-performance n-type SWCNT-TFTs, but most of them have difficulties in integration with p-type devices. For example, doping SWCNT channels with alkali metal such as potassium (K),[14] or organic polymers[15,16] such as PEI[17] and viologen[18,19] can lead to high-performance n-type TFTs. However, alkali metal and organic polymers are unstable and flowable, which may contaminate the nearby exposed p-type TFTs, which means that sparse integration is required. Another approach is covering high-κ oxide such as hafnium oxide using atomic layer deposition (ALD)[20,21] or passivation with a silicon nitride film using plasma-enhanced chemical vapor deposition

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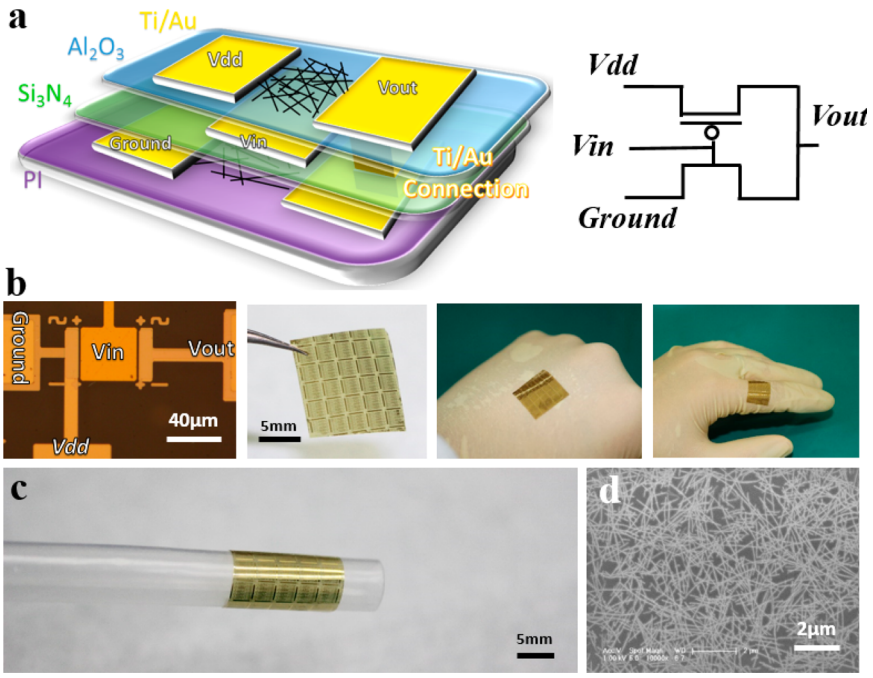

Figure 1. (a) Schematic of 3D flexible CMOS TFT inverter and its simplified circuit diagram. (b) Optical images of 3D flexible CMOS inverter arrays based on CNT-TFTs formed on polyimide substrate. (c) 3D flexible circuit functioning under a very small bending radius. (d) As-deposited SWCNT random network.

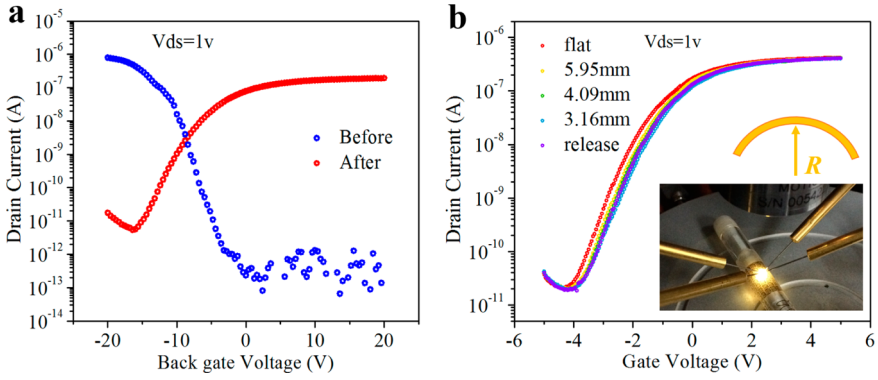

Figure 2. Fabrication of n-type CNT-TFTs. (a) Electrical properties of a CNT-TFT on the silicon dioxide substrate before and after a silicon nitride thin film was deposited on top of the channel material CNT network through PECVD (L = 20 μm, W = 100 μm); the growth conditions were 300 °C with antecedent nitrogen flow. (b) Flexible test of the n-type TFT on PI substrate under various bending radii.

(PECVD)[22,23] as the dielectric layer to isolate oxygen and water, as well as electron doping.[24] However, because the covering materials are all compact and grown at a relatively high temperature beyond the photoresist endurance, the positions of the dopant have to be defined using a relatively large size shadow mask instead of standard photolithography, leading to jumbo size devices as a result. Therefore, a method of integrating n-type and p-type TFTs compactly, massively, and stably is required. To accomplish this, three-dimensional (3D) layer-by-layer assemblies of semiconducting nanowires or SWCNTs for electronic devices or flexible devices have been studied and fabricated;[25−27] these methods provide a possible solution to the integration problem.[28,29]

Thus, in this work, we propose and fabricate flexible SWCNT-TFT CMOS circuits with 3D structure based on a two-layer stack of SWCNT networks, as Figure 1a shows. Silicon nitride grown by PECVD was used as the dielectric layer to form n-type TFTs, and p-type TFTs were constructed directly above them to compose the CMOS circuit. This strategy can overcome the patterning and lift-off problem, with only the need to etch through-holes. As a result, this method is able to save at least half of the area, make individual TFTs smaller, and integrate CMOS circuits more compactly. We also manufactured the same structure on polyimide (PI) substrates to obtain high-performance 3D flexible logic circuits such as inverters, NAND, NOR logic gates, and ring oscillators, which show excellent and stable electrical properties at various bending radii.

RESULTS AND DISCUSSION

To avoid the influence of water penetration through the backside of the substrate, 30 nm thick alumina (Al_2O_3) was grown through ALD at first, for smoothing and fixing the PI substrate as well as protecting it from oxygen and water because they could penetrate from the rear of the PI and affect the performance of the n-type TFTs.[30] Then, a uniform SWCNT

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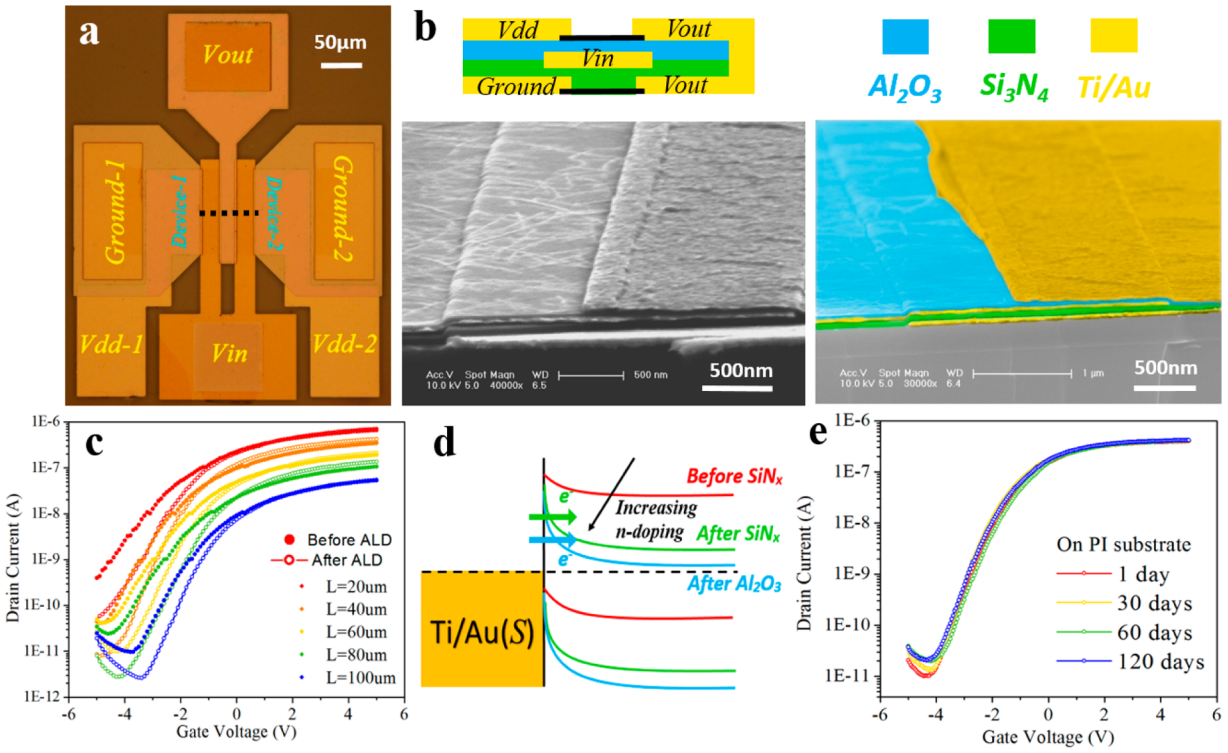

Figure 3. (a) Optical microscope photograph of two 3D flexible CMOS inverters (W = 100 μm, L = 20 μm) sharing one output electrode. (b) Cross-sectional SEM view of 3D flexible CMOS inverter, from which we can see SWCNT networks (left) and layer-by-layer structure (right) clearly. (c) Transfer curves change after growing 30 nm alumina using ALD with different channel lengths. (d) Schematic energy band diagram under on-state showing increasing n-doping after ALD of alumina. (e) Flexible n-type TFT transfer curves tested for various times.

network[31−33] was fabricated on the substrate, as described in Methods and shown in Figure 1d. A more stable and controllable compact dielectric layer was selected to realize n-type CNT-TFTs. Then, 50 nm of silicon nitride was grown through PECVD as the dielectric layer to convert the as-fabricated p-type CNT-TFTs to n-type CNT-TFTs. Actually, both HfO_2 and Si_3N_4, or even other similar dielectric materials, can be used here to realize n-type TFTs as we have been mentioned in the introduction. Here, we choose Si_3N_4 just because it can be fabricated by PECVD method, which is a reliable and easy process route[23] and the growth rate, uniformity, and repeatability are more reliable in our lab. Figure 2a shows that a high-performance n-type CNT-TFT could be obtained from p-type CNT-TFT after depositing a thin film of silicon nitride on top of the channel area, with a channel length of 20 μm and width of 100 μm. The silicon nitride thin film deposition conditions were 70 sccm (standard-state cubic centimeters per minute) nitrogen, 4 sccm silane at 300 °C, and most importantly, it was necessary to purge the chamber with nitrogen gas continuously for 30 min at 300 °C before the deposition procedure started.[34] This procedure ensured that no adsorption of water vapor and oxygen on carbon nanotubes occurred.[35] More details can be found in the Supporting Information. We also fabricated n-type TFTs on the flexible PI substrate to test their properties when curved. We measured the TFTs' electrical properties at bending radii of 5.95 mm, 4.09 mm, and 3.16 mm and found that their transfer curves had almost no change, as Figure 2b shows. Meanwhile, there was almost no TFT had electrical leakage, even at a bending radius of 3.16 mm. Thus, silicon nitride grown through PECVD is a reliable dielectric material for n-type flexible CNT-TFTs.

After the preparation of good performance n-type flexible CNT-TFTs, integrating them with the p-type TFTs is still an urgent need to be solved. As we mentioned before, because of various problems raised when fabricating n-type CNT-TFT devices, current CMOS circuits based on both p-type and n-type CNT-TFTs all have either large sizes[22,39] or large intervals.[15,19] Thus, they can only meet the requirements of large devices and the integration of p-type and n-type TFTs is inefficient and unstable as device size decreases. Here, the 3D structured CMOS circuit based on two-layer CNT-TFT devices can help to solve the problem of integrating CNT-TFT CMOS circuits. The p-type TFTs were fabricated on top of n-type top-gated TFTs. A 30 nm alumina thin film was fabricated as the dielectric layer and also the separation layer of the two-layer device using ALD after the fabrication of n-type CNT-TFTs. Then, a SWCNT thin film was deposited on it according to the Methods or transferred a ready-made thin film onto it using the method discussed in our previous work[6] as a conductive channel. After that, through-holes were defined by photolithography and the alumina dielectric layer was etched to ensure the n-type TFTs' drain electrodes exposed. Finally, source and drain electrodes and channels of the upper p-type TFTs were patterned and fabricated just above the n-type ones. In this way, we fabricated the 3D CMOS CNT-TFT circuits.

For a typical inverter, the p-type TFT was built just above the n-type TFT, using the local top gate of the n-type TFT device as the back gate of the p-type TFT device, while etching and connecting a through-hole to connect the drain electrodes of both upper p-type and lower n-type TFT devices as the V_{out} electrode. This scheme helps prevent the problem associated with planar design, in which an etching process to expose the SWCNT networks to ambient atmosphere is unavoidable for

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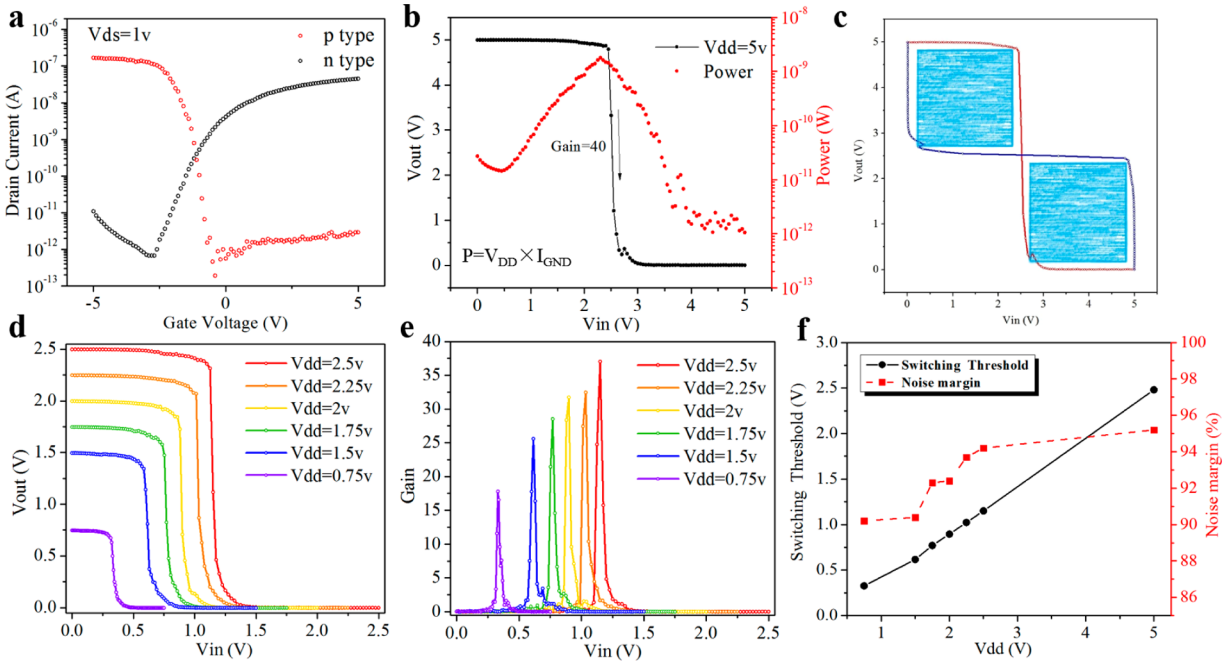

Figure 4. Electrical performance of 3D flexible CMOS inverter. (a) Typical n-type and p-type transfer curves with local gate (W = 100 μm, L = 20 μm). (b) Voltage transfer and power consumption curve at V_{dd} = 5 V, showing large gain and low power consumption. (c) VTC and corresponding "eye" pattern for noise margin extraction of 3D flexible CMOS inverter at V_{dd} = 5 V. (d) Voltage transfer curves and (e) inverter gain with supply voltage (V_{dd}) ranging from 0.75 to 2.5 V. (f) Switching threshold and total noise margin of the 3D flexible CMOS inverter under various supply voltages.

patterning n-type-TFT and p-TFT devices after dielectric growth process. However, such an etching process is unstable because wet etching may violate the back dielectric layer of p-type devices, whereas dry etching may break the SWCNTs in the channel. As a result, high-performance CMOS circuits can be established using this 3D scheme, avoiding the lift-off or etching problems and enabling smaller size devices integrated together to save at least half of the area, while improving integration density and extending the lifetime of n-type TFTs. Moreover, a more complex CMOS logic circuit must be made up of a pull-up network (PUN) and a pull-down network (PDN), where the PUN consists of p-type TFTs (on the upper layer), whereas the PDN consists of n-type TFTs (on the lower layer). Therefore, we can design the PUN and PDN respectively in their own layer and etch one or several through-holes to connect the upper and lower V_{out} electrodes (as Figure S2 shows), which is convenient for design and manufacture, ignoring the doping types in the same plane.

To observe the 3D structure directly, an inverter was cut across its conductive channel along the dotted line shown in Figure 3a. Figure 3b shows cross-sectional views of both the schematic and SEM images, from which we can see that the upper and lower source drain electrodes and middle gate electrode are separated by two dielectric layers, wherein the gate and source/drain have a small overlap to fully modulate the conductive channel. Furthermore, we can see the p-type TFT's SWCNT thin film channel clearly exposed from the undyed SEM photograph.

To achieve reliable integration of multilayer devices, it is required that the fabrication process of the upper layer device does not affect the electrical properties of the lower layer device. Here, we find that the electrical properties of the n-type TFTs not only are unaltered but also can be improved after growing alumina through ALD as the dielectric layer for p-type devices. Figure 3c shows that the on/off ratio and transconductance of n-type TFTs increase, whereas the subthreshold swing decrease after alumina deposition, where the dotted lines are before and the hollow-dotted lines are after alumina coverage. This occurs primarily because oxygen and water vapor are removed further after another high temperature and vacuum growth process. Meanwhile, alumina grown through ALD introduces more positive fixed charges, which can regulate the energy band downward and shift the transfer characteristics toward more negative gate voltages,[21,23] as well as narrowing the Schottky barrier to the conduction band to allow electron tunneling from contacts into nanotubes under the on-state, as shown in Figure 3d. In addition, ALD alumina is very dense to protect the n-type TFTs from air; similar to ALD alumina grown on the PI substrate previously, it can package the n-type TFTs entirely to prolong its life. The n-type TFTs we made on the PI substrate could work well for more than 4 months, and on the silica substrate, for 12 months, as shown in Figure 3e. Additionally, we also verified that there has almost no change of the electrical performance for the n-type TFT after the fabrication of the upper CNT channel and S/D electrodes compared with its performance just after the deposition of 30 nm alumina using ALD as shown in Figure S7, and because of the shielding effect of the middle gate electrode, there is no influence on the lower n-type TFT after adding supply voltage to the upper p-type TFT.

Figure 4a shows typical n-type and p-type CNT-TFT transfer curves under local gate modulation, and hysteresis of p-type and n-type SWCNT-TFTs are shown in Figure S4. The average on/off ratio of n-type TFTs is over 10^4, and this value is over 10^5 for p-type TFT devices, while the average subthreshold swing is near 250 mV/dec for n-type TFT devices and 170 mV/dec for p-type TFT devices. The average mobility of n-

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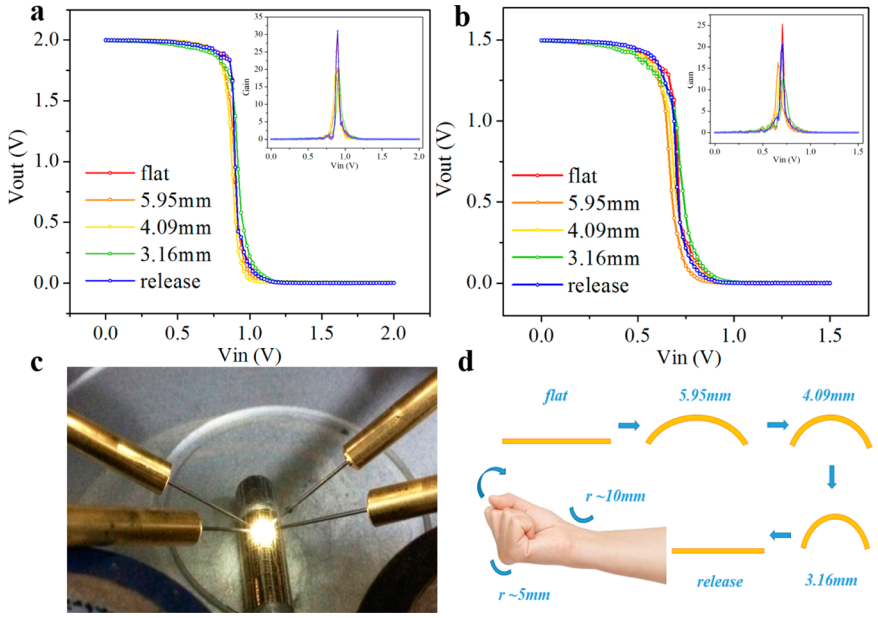

Figure 5. Flexible and wearable test. 3D flexible CMOS inverter voltage transfer curve and gain with various bending radii, working at V_{dd} of (a) 2.0 V and (b) 1.5 V. (c) Flexible test with different bending radii. (d) Minimum bending radius can meet the needs of human hand wearable devices.

type TFT devices is approximately 9 $cm^2/(V{\cdot}s)$, whereas it is over 15 $cm^2/(V{\cdot}s)$ for p-type TFT devices.

Experimental results also demonstrate that the 3D flexible CNT-TFT CMOS inverter has excellent electrical and mechanical properties. Normally, it is very important for CMOS inverters to have high gain, large noise margin (NM), low static power consumption, and exactly matched input and output voltage. The voltage transfer characteristics (VTC) and power consumption curve ($P = V_{dd}{\cdot}I_{GND}$) of a typical 3D CMOS inverter are shown in Figure 4b, in which we can see that when input voltage is varied from 0 to 5 V, the output voltage changed exactly from 5 to 0 V, which ensures the devices can be cascaded. The inverter gain is near 40, and the switching threshold is near 2.5 V, half of the "high" output voltage (5 V). Therefore, the 3D CMOS inverter has an extremely outstanding noise margin, as the eye pattern in the folded transfer curve in Figure 4c shows. Static power consumption is as low as a nanowatt, even working at the switching threshold voltage. Experimental results also show that 3D flexible CMOS inverters can work well in a wide voltage range, from 0.75 to 5 V or more. Figure 4d and e show the inverter VTC and gain under various supply voltages (V_{dd} = 0.75, 1.5, 1.75, 2, 2.25, and 2.5 V). From these results, we can see that the switching thresholds at various supply voltages are all just near half of the supply voltages, demonstrating that the inverter works in a symmetric operating voltage window, ensuring large noise margin and keeping the inverter gain at a high level, larger than 18 even when the supply voltage is reduced to 0.75 V. Meanwhile, the inverter gain shows a linear relationship with supply voltage, and this phenomenon can be explained by the theory that when V_{dd} decreases to the threshold voltage, the device's transconductance increases as V_{dd} grows, so the inverter gain increases as well.[36] In addition, we also extract and calculate the switching threshold and total noise margin ($(NM_L + NM_H)/V_{dd}$)[37] as a function of V_{dd}, as Figure 4f shows. The slope of the switching threshold voltage versus V_{dd} is close to 0.5, and the total noise margin of the inverter increases as V_{dd} grows, from 90% to 95.2%, which shows the large tolerance of the device to intrinsic or extrinsic noise.

It is an interesting phenomenon that an inverter with not totally symmetrical p-type and n-type TFT transfer and output curves (Figure S3a) can achieve a high-performance voltage transfer curve. Therefore, an aborative study of its quiescent operating characteristic was performed in detail (shown in Supporting Information). As a result, we conclude that the n-type TFT meets the velocity−saturation model and the p-type TFT meets the constant-mobility model,[38] whereas their asymmetric output curves show reduced power consumption and very good inverter voltage transfer characteristics.

We evaluated the flexibility of the 3D CMOS inverters on the PI substrate by bending the devices at different radii and investigating their electrical performance. The bending radii were 5.95 mm, 4.09 mm, and 3.16 mm, which were smaller than the minimum bending radius of human hands, as Figure 5d shows. The inverter could still work at various supply voltages, and although its gain changed a little and its switching threshold swung slightly, it still showed high performance with respect to gain and noise margin, having almost no influence for practical application. This was consistent with the slight threshold voltage change when bending the n-type TFTs, as shown above. To verify the 3D flexible CMOS circuits' resistance to bending fatigue, we also test the electrical performance of the n-type CNT-TFTs and inverters after various bending cycles over 1000 times under bending radius less than 4 mm, as Figure S5 shows, from which we can conclude that the devices could endure multiple high bending strength and keep at a high level of electrical performance. On the other hand, because the PI substrate is extremely thin, it can closely fit on various surfaces easily. With the logic stability of the 3D CMOS inverters fabricated on it, it is acceptable for flexible and wearable electronic device applications.

On the basis of the excellent electrical performance of the 3D flexible CNT CMOS inverters and the PUN and PDN model

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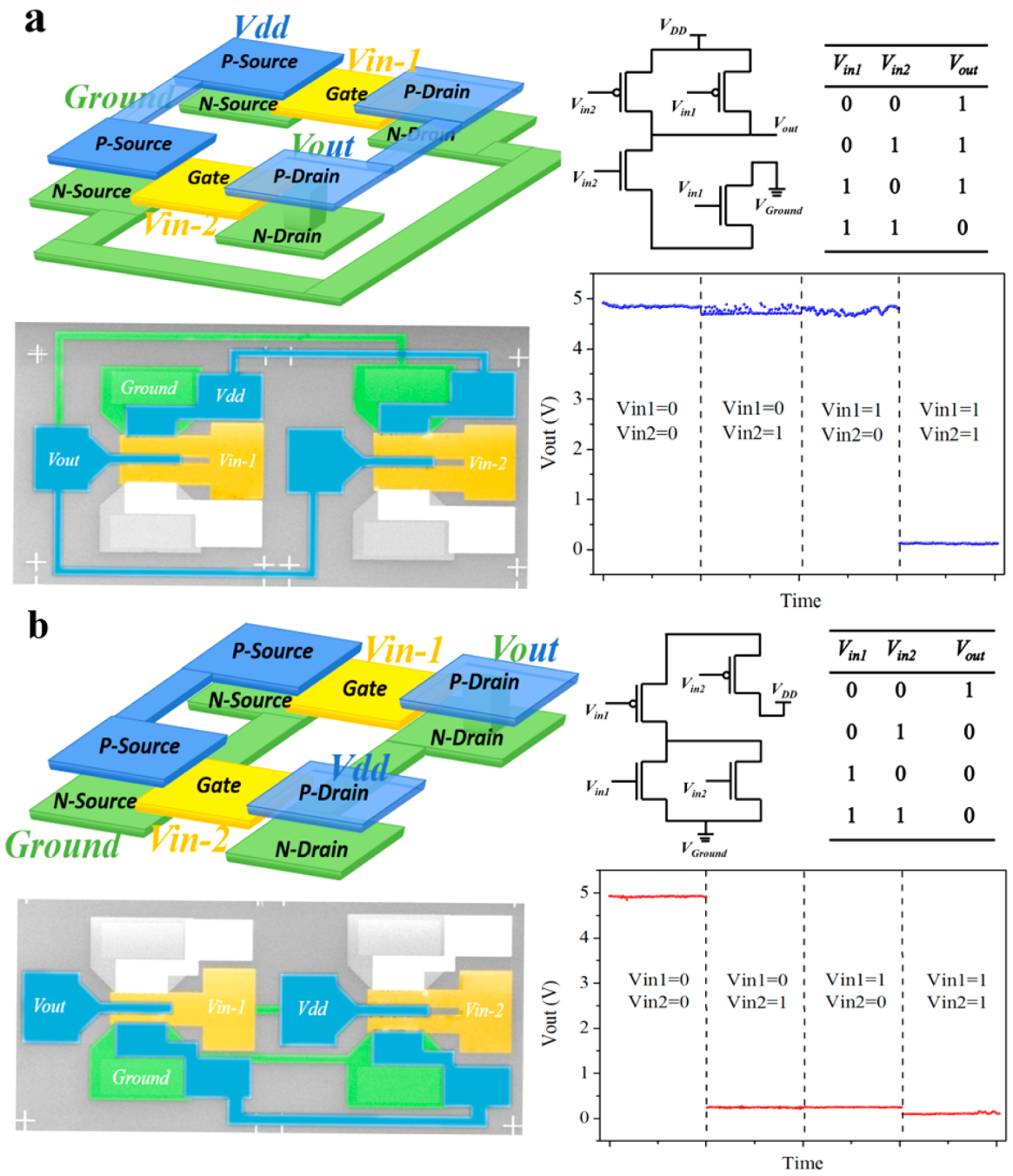

Figure 6. 3D flexible CMOS logic gates. 3D schematics, circuit diagrams, SEM images, and output performance of (a) CMOS NAND and (b) CMOS NOR logic circuits.

mentioned above, we also fabricated 3D flexible CMOS NAND and NOR logic gates. Both of them were fabricated with four TFTs, including two n-type TFTs and two p-type ones. P-type and n-type devices were isolated from up and down layers, only connected with a through-hole on the V_{out} electrode. These logic gates showed great reliability and stability. The output characteristics of these logic units are shown in Figure 6a and b, respectively. For example, for the NAND gate, when one or both inputs applied 0 V for logic "0", the output voltage ranged from 4.8 to 5 V as logic "1", when one or both inputs applied 5 V as logic "1", the output ranged from 0 to 0.3 V as logic "0".

In addition, more complex 3D flexible CMOS 15-stage ring oscillators were fabricated on the PI substrate. Figure 7a shows two nested 15-stage oscillators sharing the same output electrode; the size of each TFT is 40 μm × 40 μm. The electrode schematic in Figure 7b is the basic element of the 3D CMOS ring oscillator with two inverters, in which the parts with the same color represent connected electrodes. Figure 7c shows the typical output voltage curve of a 15-stage ring oscillator at V_{dd} = 5 V; the delay time of a single TFT is 43.85 μs, on the same order as previously reported CNT-TFT oscillators.[9,22,39−41]

Because the 3D CMOS inverter can work in a wide voltage range, the ring oscillator can also oscillate in a wide range. We found that as the supply voltage increases, the oscillation frequency increases as well, as shown in Figure 7d. This is mostly due to the growth of drain current, leading to higher switching speed and frequency when the drain voltage

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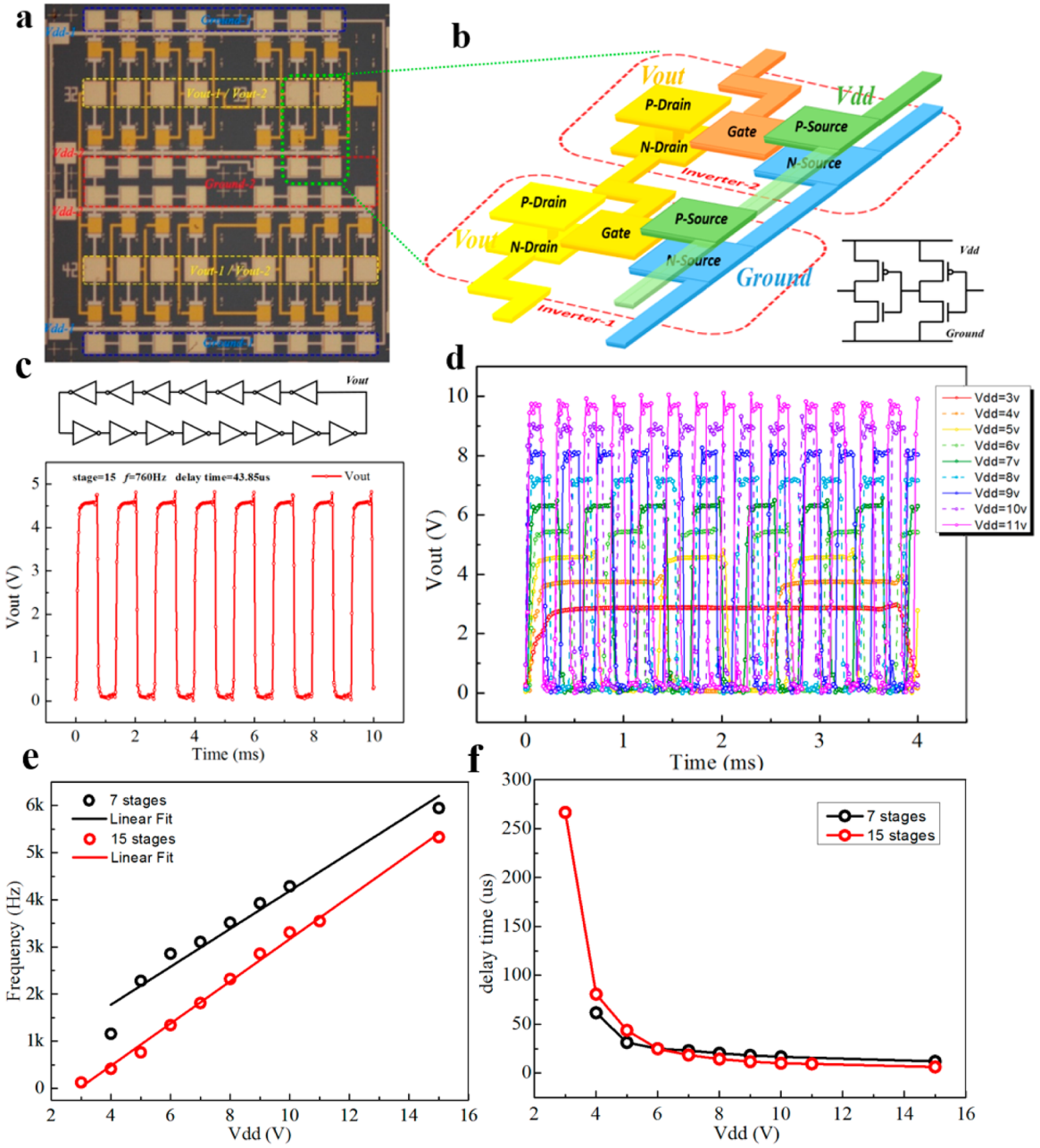

Figure 7. 3D flexible CMOS 15-stage ring oscillator. (a) Optical microscope photo of the two nested 3D CMOS ring oscillators. (b) Schematic of basic elements of 3D CMOS ring oscillator with two inverters. (c) Typical output voltage of the 3D flexible CMOS ring oscillator at V_{dd} = 5 V. (d) Output voltage of 3D flexible CMOS ring oscillator with various supply voltages. (e) Oscillation frequency increases linearly with supply voltage, for 15-stage rings and 7-stage rings separately. (f) Delay time changes with supply voltage.

increases. Figure 7e shows the plot of oscillation frequency versus supply voltage and the fitting curves of 15-stage and 7-stage oscillators. The oscillation frequency of both devices shows a linear relationship with supply voltage. Output voltage oscillograms of the 7-stage oscillator and oscillogram under V_{dd} = 15 V of the 15-stage oscillator can be found in Supporting Information Figure S6.

We can calculate the delay time of each TFT using the formula $t = 1/(2Nf)$, in which N is the stage of the ring oscillator and f is its frequency at a specific supply voltage.[42] Then, we obtain the relationship between delay time and V_{dd}, as shown in Figure 7f. When the supply voltage is high enough for the ring oscillator to work in favorable conditions, which means in this voltage range (5 V or more in Figure 7f), the variation of delay time is insensitive as supply voltage changes and could be kept in a relatively small range, the ring oscillator can endure larger noise and work more stable, whereas beyond that, as the supply voltage decreases, the delay time increases rapidly, behaving like silicon-based field-effect transistors.[36] We can use the standard first-order analysis of delay time to explain this phenomenon. The delay time is defined as the average delay of the output voltage rise and trail, as formula 1 shows, where t_{pHL} is the delay time of the trailing edge of the output voltage, and similarly, t_{pLH} is the delay time of the rising edge

$$t_p = \frac{t_{pHL} + t_{pLH}}{2} \quad (1)$$

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Because the expansion formulas of t_{pHL} and t_{pHL} are the same, we can consider only one of them to represent the change in delay time. Expanding t_{pHL} shows its relationship with V_{dd}, as in formula 2[36]

$$t_{pHL} = (\ln 2)\frac{3}{4}\frac{C_L V_{DD}}{I_{DSATn}} = 0.52\frac{C_L V_{DD}}{\left(\frac{W}{L}\right)_n k'_n V_{DSATn}\left(V_{DD} - V_{Tn} - \frac{V_{DSATn}}{2}\right)} \quad (2)$$

When V_{dd} is high enough, at $V_{dd} \gg V_{Tn} + (V_{DSATn}/2)$, t_{pHL} can be simplified as a constant, shown in formula 3

$$t_{pHL} \approx 0.52\frac{C_L}{\left(\frac{W}{L}\right)_n k'_n V_{DSATn}} \quad (3)$$

Therefore, the delay time of a single TFT is almost constant when V_{dd} is high enough. On the other hand, from formula 2, we know that if V_{dd} is sufficiently low, the delay time will increase rapidly when V_{dd} is decreased, which conforms to Figure 7f completely. Additionally, the delay time of the TFT in the 7-stage ring oscillator is almost the same as that of the 15-stage ring oscillator, which confirms that the 3D CMOS is a reliable architecture that leads to repeatable performance and uniform units; thus, it is suitable for application in complex flexible and wearable electronic devices.

CONCLUSIONS

In summary, we have proposed and fabricated stable and repeatable flexible CNT-TFT CMOS integrated circuits based on a 3D structure. Two layers of CNT-TFT devices were stacked, where one layer served as n-type devices and the other layer served as p-type devices. The n-type CNT-TFTs were realized by depositing silicon nitride thin film as the dielectric layer modulated with top gates. The p-type CNT-TFTs were located on top of the n-type devices and were locally back gated, with the channel CNTs exposed. To a certain extent, this fabrication process solved the main problems associated with SWCNT-based CMOS integration, such as fluidity and volatility for liquid organic polymers, and inability to lift-off for the compact dielectric layer. This method was able to save at least half of the area required to construct an inverter, improve n-type TFT performance, prolong its life to more than four months, and integrate CMOS circuits more compactly. 3D flexible CMOS NOR and NAND logic gates and 15-stage ring oscillators were fabricated on PI substrates with high performance. Stable electrical properties for CMOS inverters could be obtained with a bending radius as small as 3.16 mm, which showed that this 3D structure is a reliable architecture and suitable for electrical application of SWCNTs in complex flexible and wearable electronic devices.

METHODS

Deposition of SWCNT Thin Films. SWCNTs were purchased from NanoIntegris Inc. in powder form with a semiconductor purity of 99%, mean diameter of 1.4 nm, and an average length of 1.8 μm. Then, the powder was dispersed in *N*-methyl-2-pyrrolidone (Sigma-Aldrich) using horn sonication for preparing to deposit to the target substrate. SWCNT thin films could both be transferred[6] or directly deposited onto PI substrates. For direct deposition, polyimide (Foxconn) with a thickness of 25 μm was tiled on 300 nm thermal SiO_2 on a p^{++} Si substrate, and ALD was used to deposit a layer of 30 nm Al_2O_3 to fix the PI substrate and protect it. Al_2O_3 was grown at 120 °C using trimethylaluminum and water as the precursors. Then, to functionalize the oxide surface, O_2 plasma etching was employed to make it hydrophilic, and the samples were immersed in isopropanol (IPA)-diluted aminopropyltriethoxysilane (APTES, Sigma-Aldrich) solution (IPA:APTES = 1:20) for 30 min and then rinsed with IPA. Subsequently, the samples were immersed into the semiconducting nanotube solution for several hours to deposit SWCNT random network thin films.

Fabrication of Devices. Electrodes, test holes, and conductive channels were defined by standard photolithography. All electrodes contained 5 nm Ti as an adhesive coating and 50 nm Au, and conductive channels were patterned through O_2 plasma etching. Test holes through silicon nitride were etched by CF_4 plasma etching, whereas BCl_3 with Cl_2 plasma etching was used for Al_2O_3 test holes.

Characterization of Electrical Properties. N-type and 3D inverter electrical measurements were performed with a semiconductor analyzer (4156C, Agilent, U.S.A.) with a probe station (Lakeshore, U.S.A.) in ambient atmosphere at room temperature. The flexible tests were developed by pasting the PI substrate to a mold closely and using the same semiconductor analyzer with a different probe station (EverBeing, Taiwan) to measure electrical properties under various bending radii. The output voltage of the ring oscillators was acquired by a digital oscilloscope (TDS2012C, Tektronix, U.S.A.).

ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge on the ACS Publications website at DOI: 10.1021/acsnano.5b06726.

The influence of silicon nitride deposition conditions on the properties of n-type CNT-TFTs (S1), pull-up network (PUN) and pull-down network (PDN) units in a CMOS circuit fabricated on upper and lower layers, separately (S2), working principle of the 3D flexible CMOS inverter (S3), hysteresis of p-type and n-type SWCNT TFTs (S4), fatigue test of the n-type SWCNT TFT and the 3D CMOS inverter (S5), 7-stage oscillator's output voltage oscillograms and 15-stage oscillator's oscillogram under V_{dd} = 15 V (S6), electrical performance of the n-type CNT-TFT during manufacturing processes (S7). (PDF)

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Notes

The authors declare no competing financial interest.

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REFERENCES

(1) Fuhrer, M. S.; Kim, B. M.; Dürkop, T.; Brintlinger, T. High-Mobility Nanotube Transistor Memory. *Nano Lett.* **2002**, *2*, 755−759.
(2) Yao, Z.; Kane, C. L.; Dekker, C. High-Field Electrical Transport in Single-Wall Carbon Nanotubes. *Phys. Rev. Lett.* **2000**, *84*, 2941−2944.

DOI: 10.1021/acsnano.5b06726
ACS Nano 2016, 10, 2193−2202

(3) Bozovic, D.; Bockrath, M.; Hafner, J. H.; Lieber, C. M.; Park, H.; Tinkham, M. Plastic Deformations in Mechanically Strained Single-Walled Carbon Nanotubes. *Phys. Rev. B: Condens. Matter Mater. Phys.* **2003**, *67*, 033407/1−4.
(4) Xu, F.; Wu, M. Y.; Safron, N. S.; Roy, S. S.; Jacobberger, R. M.; Bindl, D. J.; Seo, J. H.; Chang, T. H.; Ma, Z.; Arnold, M. S. Highly Stretchable Carbon Nanotube Transistors with Ion Gel Gate Dielectrics. *Nano Lett.* **2014**, *14*, 682−686.
(5) Lau, P. H.; Takei, K.; Wang, C.; Ju, Y.; Kim, J.; Yu, Z.; Takahashi, T.; Cho, G.; Javey, A. Fully Printed, High Performance Carbon Nanotube Thin-Film Transistors on Flexible Substrates. *Nano Lett.* **2013**, *13*, 3864−3869.
(6) Zou, Y.; Li, Q.; Liu, J.; Jin, Y.; Qian, Q.; Jiang, K.; Fan, S. Fabrication of All-Carbon Nanotube Electronic Devices on Flexible Substrates through CVD and Transfer Methods. *Adv. Mater.* **2013**, *25*, 6050−6056.
(7) Aguirre, C. M.; Levesque, P. L.; Paillet, M.; Lapointe, F.; St-Antoine, B. C.; Desjardins, P.; Martel, R. The Role of the Oxygen/Water Redox Couple in Suppressing Electron Conduction in Field-Effect Transistors. *Adv. Mater.* **2009**, *21*, 3087−3091.
(8) Qian, Q.; Li, G.; Jin, Y.; Liu, J.; Zou, Y.; Jiang, K.; Fan, S.; Li, Q. Trap-State-Dominated Suppression of Electron Conduction in Carbon Nanotube Thin-Film Transistors. *ACS Nano* **2014**, *8*, 9597−9605.
(9) Sun, D. M.; Timmermans, M. Y.; Tian, Y.; Nasibulin, A. G.; Kauppinen, E. I.; Kishimoto, S.; Mizutani, T.; Ohno, Y. Flexible High-Performance Carbon Nanotube Integrated Circuits. *Nat. Nanotechnol.* **2011**, *6*, 156−161.
(10) Cao, Q.; Kim, H. S.; Pimparkar, N.; Kulkarni, J. P.; Wang, C.; Shim, M.; Roy, K.; Alam, M. A.; Rogers, J. A. Medium-Scale Carbon Nanotube Thin-Film Integrated Circuits on Flexible Plastic Substrates. *Nature* **2008**, *454*, 495−500.
(11) Tsai, C. L.; Xiong, F.; Pop, E.; Shim, M. Resistive Random Access Memory Enabled By Carbon Nanotube Crossbar Electrodes. *ACS Nano* **2013**, *7*, 5360−5366.
(12) Someya, T.; Small, J.; Kim, P.; Nuckolls, C.; Yardley, J. T. Alcohol Vapor Sensors Based on Single-Walled Carbon Nanotube Field Effect Transistors. *Nano Lett.* **2003**, *3*, 877−881.
(13) Shulaker, M. M.; Hills, G.; Patil, N.; Wei, H.; Chen, H. Y.; Wong, H. S.; Mitra, S. Carbon Nanotube Computer. *Nature* **2013**, *501*, 526−530.
(14) Ryu, K.; Badmaev, A.; Wang, C.; Lin, A.; Patil, N.; Gomez, L.; Kumar, A.; Mitra, S.; Wong, H. S.; Zhou, C. CMOS-Analogous Wafer-Scale Nanotube-on-Insulator Approach for Submicrometer Devices and Integrated Circuits Using Aligned Nanotubes. *Nano Lett.* **2009**, *9*, 189−197.
(15) Wang, H.; Wei, P.; Li, Y.; Han, J.; Lee, H. R.; Naab, B. D.; Liu, N.; Wang, C.; Adijanto, E.; Tee, B. C.; Morishita, S.; Li, Q.; Gao, Y.; Cui, Y.; Bao, Z. Tuning the Threshold Voltage of Carbon Nanotube Transistors by N-Type Molecular Doping for Robust and Flexible Complementary Circuits. *Proc. Natl. Acad. Sci. U. S. A.* **2014**, *111*, 4776−4781.
(16) Wang, H.; Li, Y.; Jimenez-Oses, G.; Liu, P.; Fang, Y.; Zhang, J.; Lai, Y.; Park, S.; Chen, L.; Houk, K. N.; Bao, Z. N-Type Conjugated Polymer-Enabled Selective Dispersion of Semiconducting Carbon Nanotubes for Flexible CMOS-Like Circuits. *Adv. Funct. Mater.* **2015**, *25*, 1837−1844.
(17) Duan, Y.; Holmes, N. E.; Ellard, A. L.; Gao, J.; Xue, W. Solution-Based Fabrication and Characterization of a Logic Gate Inverter Using Random Carbon Nanotube Networks. *IEEE Trans. Nanotechnol.* **2013**, *12*, 1111−1117.
(18) Lee, S. Y.; Lee, S. W.; Kim, S. M.; Yu, W. J.; Jo, Y. W.; Lee, Y. H. Scalable Complementary Logic Gates with Chemically Doped Semiconducting Carbon Nanotube Transistors. *ACS Nano* **2011**, *5*, 2369−2375.
(19) Geier, M. L.; Prabhumirashi, P. L.; McMorrow, J. J.; Xu, W.; Seo, J. W.; Everaerts, K.; Kim, C. H.; Marks, T. J.; Hersam, M. C. Subnanowatt Carbon Nanotube Complementary Logic Enabled by Threshold Voltage Control. *Nano Lett.* **2013**, *13*, 4810−4814.
(20) Javey, A.; Kim, H.; Brink, M.; Wang, Q.; Ural, A.; Guo, J.; McIntyre, P.; McEuen, P.; Lundstrom, M.; Dai, H. High-Kappa Dielectrics for Advanced Carbon-Nanotube Transistors and Logic Gates. *Nat. Mater.* **2002**, *1*, 241−246.
(21) Zhang, J.; Wang, C.; Fu, Y.; Che, Y.; Zhou, C. Air-Stable Conversion of Separated Carbon Nanotube Thin-Film Transistors from p-Type to n-Type Using Atomic Layer Deposition of High-κ Oxide and Its Application in CMOS Logic Circuits. *ACS Nano* **2011**, *5*, 3284−3292.
(22) Gao, P. Q.; Zou, J. P.; Li, H.; Zhang, K.; Zhang, Q. Complementary Logic Gate Arrays Based on Carbon Nanotube Network Transistors. *Small* **2013**, *9*, 813−819.
(23) Ha, T. J.; Chen, K.; Chuang, S.; Yu, K. M.; Kiriya, D.; Javey, A. Highly Uniform and Stable N-Type Carbon Nanotube Transistors by Using Positively Charged Silicon Nitride Thin Films. *Nano Lett.* **2015**, *15*, 392−397.
(24) Suriyasena Liyanage, L. L.; Xu, X.; Pitner, G.; Bao, Z.; Wong, H. S. VLSI-Compatible Carbon Nanotube Doping Technique with Low Work-function Metal Oxides. *Nano Lett.* **2014**, *14*, 1884−1890.
(25) Javey, A.; Nam, S.; Friedman, R. S.; Yan, H.; Lieber, C. M. Layer-by-Layer Assembly of Nanowires for Three-Dimensional, Multifunctional Electronics. *Nano Lett.* **2007**, *7*, 773−777.
(26) Ahn, J.-H.; Kim, H.-S.; Lee, K. J.; Jeon, S.; Kang, S. J.; Sun, Y.; Nuzzo, R. G.; Rogers, J. A. Heterogeneous Three-Dimensional Electronics by Use of Printed Semiconductor Nanomaterials. *Science* **2006**, *314*, 1754−1757.
(27) Yamada, T.; Makiomoto, N.; Sekiguchi, A.; Yamamoto, Y.; Kobashi, K.; Hayamizu, Y.; Yomogida, Y.; Tanaka, H.; Shima, H.; Akinaga, H.; Futaba, D. N.; Hata, K. Hierarchical Three-Dimensional Layer-by-Layer Assembly of Carbon Nanotube Wafers for Integrated Nanoelectronic Devices. *Nano Lett.* **2012**, *12*, 4540−4545.
(28) Nam, S.; Jiang, X.; Xiong, Q.; Ham, D.; Lieber, C. M. Vertically Integrated, Three-Dimensional Nanowire Complementary Metal-Oxide-Semiconductor Circuits. *Proc. Natl. Acad. Sci. U. S. A.* **2009**, *106*, 21035−21038.
(29) Honda, W.; Harada, S.; Ishida, S.; Arie, T.; Akita, S.; Takei, K. High-Performance, Mechanically Flexible, and Vertically Integrated 3D Carbon Nanotube and InGaZnO Complementary Circuits with a Temperature Sensor. *Adv. Mater.* **2015**, *27*, 4674−4680.
(30) MacDonald, W. A.; Looney, M. K.; MacKerron, D.; Eveson, R.; Adam, R.; Hashimoto, K.; Rakos, K. Latest Advances in Substrates for Flexible Electronics. *J. Soc. Inf. Disp.* **2007**, *15*, 1075−1083.
(31) Wang, C.; Zhang, J.; Ryu, K.; Badmaev, A.; De Arco, L. G.; Zhou, C. Wafer-Scale Fabrication of Separated Carbon Nanotube Thin-Film Transistors for Display Applications. *Nano Lett.* **2009**, *9*, 4285−4291.
(32) Zhang, J.; Fu, Y.; Wang, C.; Chen, P.; Liu, Z.; Wei, W.; Wu, C.; Thompson, M. E.; Zhou, C. Separated Carbon Nanotube Macro-electronics for Active Matrix Organic Light-Emitting Diode Displays. *Nano Lett.* **2011**, *11*, 4852−4858.
(33) Wang, C.; Chien, J. C.; Takei, K.; Takahashi, T.; Nah, J.; Niknejad, A. M.; Javey, A. Extremely Bendable, High-Performance Integrated Circuits Using Semiconducting Carbon Nanotube Networks for Digital, Analog, and Radio-Frequency Applications. *Nano Lett.* **2012**, *12*, 1527−1533.
(34) Li, H.; Zhang, Q.; Liu, C.; Xu, S.; Gao, P. Ambipolar to Unipolar Conversion in Graphene Field-Effect Transistors. *ACS Nano* **2011**, *5*, 3198−3203.
(35) Li, G.; Li, Q.; Jin, Y.; Zhao, Y.; Xiao, X.; Jiang, K.; Wang, J.; Fan, S. Fabrication of Air-Stable N-Type Carbon Nanotube Thin-Film Transistors on Flexible Substrates Using Bilayer Dielectrics. *Nanoscale* **2015**, *7*, 17693−17701.
(36) Rabaey, J. M.; Chandrakasan, A.; Nikolic, B. *Digital Integrated Circuits A Design Perspective*, 2nd ed.; Prentice Hall: Upper Saddle River, NJ, 2002.
(37) Yu, L.; Zubair, A.; Santos, E. J. G.; Zhang, X.; Lin, Y.; Zhang, Y.; Palacios, T. High-Performance WSe_2 Complementary Metal Oxide Semiconductor Technology and Integrated Circuits. *Nano Lett.* **2015**, *15*, 4928−4934.

DOI: 10.1021/acsnano.5b06726
ACS Nano 2016, 10, 2193−2202

(38) Sze, S. M.; Kwok, K. N. *Physics of Semiconductor Devices*, 3rd ed.; John Wiley and Sons: Hoboken, NJ, 2006.
(39) Xu, W.; Liu, Z.; Zhao, J.; Xu, W.; Gu, W.; Zhang, X.; Qian, L.; Cui, Z. Flexible Logic Circuits Based on Top-Gate Thin Film Transistors with Printed Semiconductor Carbon Nanotubes and Top Electrodes. *Nanoscale* **2014**, *6*, 14891−14897.
(40) Ha, M.; Xia, Y.; Green, A. A.; Zhang, W.; Renn, M. J.; Kim, C. H.; Hersam, M. C.; Frisbie, C. D. Printed, Sub-3V Digital Circuits on Plastic from Aqueous Carbon Nanotube Inks. *ACS Nano* **2010**, *4*, 4388−4395.
(41) Yoon, J.; Shin, G.; Kim, J.; Moon, Y. S.; Lee, S.-J.; Zi, G.; Ha, J. S. Fabrication of Stretchable Single-Walled Carbon Nanotube Logic Devices. *Small* **2014**, *10*, 2910−2917.
(42) Ha, M.; Seo, J. W.; Prabhumirashi, P. L.; Zhang, W.; Geier, M. L.; Renn, M. J.; Kim, C. H.; Hersam, M. C.; Frisbie, C. D. Aerosol Jet Printed, Low Voltage, Electrolyte Gated Carbon Nanotube Ring Oscillators with Sub-5 Mus Stage Delays. *Nano Lett.* **2013**, *13*, 954−960.

DOI: 10.1021/acsnano.5b06726
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